AN INTRODUCTION TO

MICROPROCESSORS

by

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playmatic

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1) INTRODUCTION

1.1.0. Basic concepts of binary logic

The purpose of this paragraph is the introduction of the basic mathematical concepts, that will allow us to work with microprocessors.
These basic concepts are: bit, numerical systems, arithmetics and logic (or boolean algebra).

1.1.1. What is a bit?

A BIT (the word is an abbreviation of binary digit) is a variable that can be 1 or 0 and note any other value.
From a technological point of vieuw, this concept is useful as a bit can be implemented by any bistable device. As an example of a device that can represent a bit, we have the switch:

From a conceptual point of view, the most important of this concept is that we can build a set of logical and arithmetical rules that allow us to perform any of the operations of a computer.

1.1.2. Representation of a number in base 10.

In the decimal numerical system, each digit is a decimal variable, that is: it can have one of the following values: Ø, 1, 2, 3, 4, 5, 6, 7, 8, 9.

When writing a number in decimal system, what we are doing is:

$$11 = (1 \times 10) + (1 \times 1)$$

$$2347 = (2 \times 1000) + (3 \times 100) + (4 \times 10) + (7 \times 1)$$

that is, the most right digit has value 1, the next value 10, the other 100, and so on. If we write it in power form, we will have: 10^0, 10^1, 10^2, 10^3,... .. and so we say that the base of the system is 10

1.1.3. Representation of a number in base 2.

In the binary system, everything works in the same way as in the decimal system with the exception of the base of the system, that in this case is 2. So, every digit in this system will be a BIT.
Example:

binary 11 = (1 x 2) + (1 x 1) = decimal 3
binary 1011 = (1x8)+ (0x4)+(1x2)+(1x1) = decimal 11

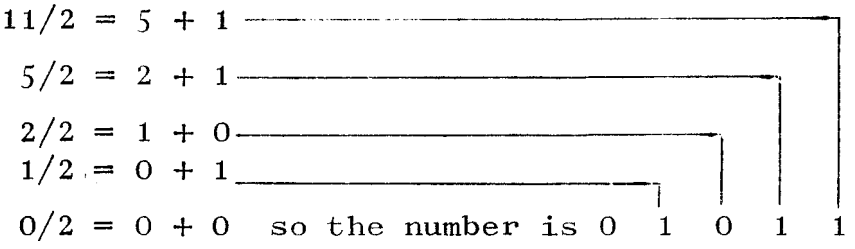
In this case the most right digit has value 1; the next, value 2 the next, 4, the next 8 and so on..... In power notation:

2^0, 2^1, 2^2, 2^3, ...

1.1.4. Conversion of a number from a base to another

An easy method to change the number from decimal to binary base consists in dividing the decimal number by 2 and take the remainders.

For example: we want to change the decimal number 11 into the binary system:



That is, decimal 11 = 1011

If the numbers we are treating with are fractions, in order to change a binary number into decimal, we must multiply by:

$2^{-1} = 1/2 = 0,5$; $2^{-2} = 1/4 = 0,25$; .....

For example, if we have 0,1011 in binary system, we must operate in the following way:

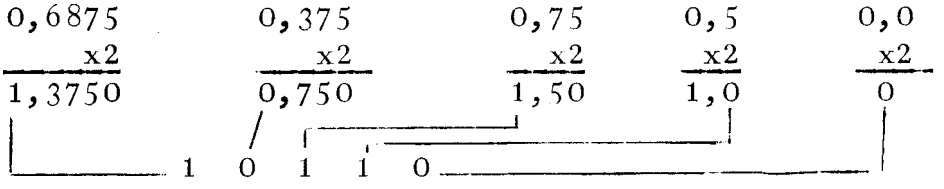
$$0,1011 = (1x2^{-1}) + (0x2^{-2}) + (1x2^{-3}) + (1x2^{-4}) =$$

$$= (1x0,5) + (0x0,25) + (1x0,125) + (1x0,0625) =$$

decimal 0,6875.

To perform the inverse conversion, we must multiply by 2 the fractional part and we take the integer part (largest integer smaller or equal than the result of the multiplication).

For example, if we have 0,6875 (decimal), we will operate in the following way:



and the decimal 0,6875 will be the binary 0,1011.

Unfortunately, the conversions binary/decimal with fractional numbers are not always exact. (by that we mean that in any of the numerical system a number that in oder can be expressed by a finite number of digits can need infinite digits).

In the same way, as a fraction like 2/3 has not exact decimal representation, a decimal fraction that is different from any finite addition of terms of the form 2^{-a}, will be an approximate binary fraction.

For example, if we have 0,42357 in decimal, to obtain its binary representation, we operate as before and attain:

0,42357	0,84714	0,69428	0,38856	0,77712
x2	x2	x2	x2	x2
0,84714	1,69428	1,38856	0,77712	1,55424
0	1	1	0	1

that is, 0,42357 will be 0,01101.... and we should continue the conversion with 0,55424.
Let us calculate the error that we have had by performing the approximation:

$$0,42357_{(10} - 0,01101_{(2}$$

In order to calculate the error, we must perform the inverse conversion:

$$0,01101 = (0x2^{-1}) + (1x2^{-2}) + (0x2^{-4}) + (1x2^{-5}) =$$

$$0,40625_{(10}$$

and the error will be:

$$E = 0,42357 - 0,40625 = 0,01732_{(10}$$

This difference is caused by the neglected reminder 0,55424
This error can also be calculated by:

$$\text{Error} = [\text{neglected reminder}] \times [\text{smaller calculated term}] = [0,55424] \times [2^{-5}] = [0,55424] \times [0,03125] = 0,01731_{(10}$$

1.1.5. Octal and hexadecimal systems

As binary numbers are quite long, although they are not great numbers, the bits are normally grouped in sets of 3 or 4 bits.
In this case we have base 8 and 16 systems respectively. These systems are called octal and hexadecimal respectively.

For example: 6 7 5 4 = 6754 (octal)
110111101100 base 2
D E C = DEC (hexadecimal

We must realize, that in the hexadecimal system, letters A, B, C, D, E and F are used to denote decimal numbers 10, 11, 12, 13, 14 and 15.

1.1.6. Binary arithmetics

With binary numbers, the same operations can be performed as with decimal numbers, following basically the same rules. In fact, binary arithmetics is much easier than decimal one.
Let us seee addition and substraction:

1.1.6. (1) Binary addition

When performing decimal additions, we have:

```
  1  1
  2  0  8
+    9  2        carry 1
-------------
  3  0  0
```

so, in binary will be:

```
  1  1
     0  1  1
+    1  1  0     carry 1
-------------
  1  0  0  1
```

1.1.6. (2) Binary substraction.

As computers are usually not able to substract numbers and they can only add them, we are going to transform substractions into additions.
In decimal system we call "complement to 10" of a number, to the result of substracting this number from 10.
For example, the complement to 10 of 2 will be :

$$10 - 2 = 8$$

Performing a substraction in the decimal system, is the same as adding the complement to 10 of the substracted to the minuend and neglecting the carry.
For example: $9 - 2 = 7$

We can do the following: "complement to 10" of $2 = 10 - 2 = 8$ and then:

```
  1
  9
+ 8        carry 1
-------
 17
```

and neglecting the carry, we obtain the correct result: 7

When working in the binary system, we need to use "the complement to 2". For doing so, we obtain the "complement to 1" and add 1.

As it is easy to see, the complement to 1 can be obtained by changing the 1's into 0's and vice versa.

For example: binary nº 0101
complement to 1 - 1010
complement to 2 - 1011

Perform a substraction in binary system is: perform the complement to 2 of the substrahend and add it to the minuend neglecting the last carry.

For example: 1 0 0 0 1
-0 1 0 1 1
0 0 1 1 0

is equivalent to:

1 0 0 0 1
- 1 0 1 0 1 — complement to 2 of
NEGLECTED 1 0 0 1 1 0

In decimal system, if the substrahend is bigger than the minuend, the result of the operation will be a negative number and we will operate as follows:

2 - 9 = -7

complement to 10 of 9 = 10 - 9 = 1

so: 0
2

+1 carry 0
03

and complement to 10 of 3 = 10 - 3 = 7 (with carry 0)

That is, the last carry will indicate if the result is negative or positive.

CARRY = { 1 = positive result
0 = negative result

If the result is positive, we obtain directly the result. If the result is negative, we must find the complement to 10 to obtain the absolute value of the result.
All this applies to the case of the binary system. (Naturally everything referred to the complement to 2)

1.1.7. Boolean algebra

Boolean algebra is very important for the applications of microcomputers. It provides the basic to take decisions, prepares conditions and many logical operations

Boolean algebra, uses bits 0 and L to define the logical decisions.
There are four elemental logical operations:

1.1.7 (1) "OR" operation (+)
The output is always 1, if any of the inputs is 1.

The truth table is:

	0	1
0	0	1
1	1	1

1.1.7.(2) "AND" operation, (•) ( ).
The output is 1 only when all the inputs are 1.

The truth table is:

	0	1
0	0	0
1	0	1

1.1.7. (3) "OR exclusive" operation (+) (-).
The output is 1 when the inputs are different and 0 when the inputs are equal.

The truth table is:

	0	1
0	0	1
1	1	0

1.1.7. (4) "NOT" operation.
This operation performs the complement to 1 of the output

$$\overline{1} = 0$$

$$\overline{0} = 1$$

1.1.8. The De Morgan theorems
Usually microcomputers only perform AND and NOT operations. The De Morgan theorems provide us the method to change OR operations into AND operations and vice versa.

The theorems are: $\overline{A}.\overline{B} = \overline{A+B}$, $\overline{A} + \overline{B} = \overline{A}.\overline{B}$

If, for example, we want to change AND into OR and NOT we have:

$$A.B = \overline{\overline{A}+\overline{B}}$$

and the same with exclusive OR.

$$A \quad B = (\overline{A}+B) + (A+\overline{B})$$

2). The MOS transistor

1.2.1.1. Bipolar transistors and MOS transistors.

Bipolar transistors are the clasical transistors with three elements and two junctions. They can be NPN or PNP. Their operation is controlled by two types of carriers: majority and minority ones, or electrons and holes.

There is another type of transistors. There are the FET's (Field Effect Transistor). The MOS is one of the most important FET transistors. In this case the current flows from source to drain. The three elements of the transistor are of the same type (P or N).

The electrode of command of the MOS transistor is electrically isolated by a thin oxide film. At the beginning this electrode was made of aluminium. Because of that, the transistor was called Metal-Oxide-Semiconductor, that is: MOS.

Today the name obsolete as the isolator is not always an oxide.

The correct name should be MIS (Metal-Isolant-Semiconductor). Anyway, as the difference is only in the terminology and the operation is the same, we are going to use the name of MOS.

1.2.1.2. Family analysis.

Actually RTL circuits and more recently DTL ones are getting obsolete, as the TTL and ECL families more and more imposed among the bipolar logic families.

The most important rival of these families is the CI/MOS. In 1970 it was used a 15%, during the period 1970-1974 it reached the 30% and actually is used approximately a 50%.

1.2.1.3. The companies.

About one hundred companies participate in the pro-durction of semi-conductors and more than 50 fabricate their integrated circuits. From these companies, less than 10 provide about the 50% of the total semi-conductor market. In 1970, the situation was as follows:

1.- "TEXAS" with a sales volume of more than 300 millions dollars.
2.- "MOTOROLA" with 300 millions
3.- "FIRCHILD" with 200 millions
4.- The "PHILIPS" group with 95 millions
5.- "ITT" with 75 millions

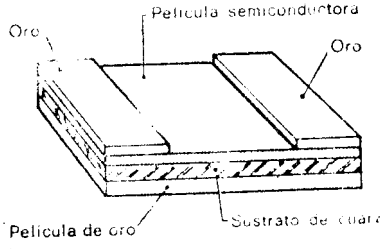
6.- "GENERAL ELECTRIC" with 60 millions
7.- "RCA" with 50 millions
8.- "NIPPON" with 50 millions

At the time there were some other with a sales volume of 40 millions dollars: SESCOSEM, SIEMENS, NATIONAL SEMICONDUCTOR & SPRAGUE.
With a sales volume of less than 40 millions dollars, we have:BURR BROWN, HEWLETT-PACKARD, INTEL, INTERSIL, MONSANTO, MOSTEK and ROCKWELL.
Because of the crisis of 1971, GENERAL ELECTRIC leaves the production of integrated circuits from october 1971.

1.2.1.4. Brief history of the MOS.

In 1930 was discovered a component that seems has the same operation as the field effect elements. This discovery was made by the american investigator Lilienfeld, who took two patents on this matter:
- 1926 U.S. Patent nº 1900018 by J.E.Lilienfeld
- 1930 U.S. Patent nº 1745175 by J.E. Lilienfeld

In 1935 the english Oscar Heil goes deeper into the theme of field effect and get the Britisch Patent nº 439457.
In 1948, Shockly discover the variations of the conductivity in thin semiconductor films under an electrical field. (fig. 1.1.)



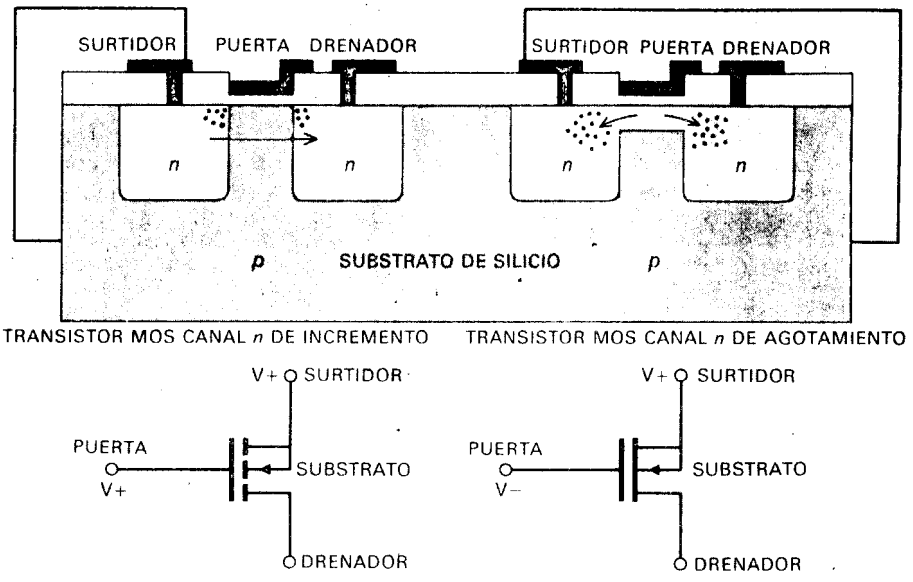
In this year at the Bell laboratories, a group of investigators directed by M.Atalià, begins to study the possibilities of the MOS as discrete component. The point of departure of the investigations are Silicon and Silicon dioxide.
Hofstein and Heiman develop the first MOS device that can be produced in mass. Heiman obtains an RCA Patent for an enhancement MOS and Hofstein patents the future double gate MOS.
In 1959, J.Torkel Wallmark of RCA, sees the possibility of implmenting logical functions with MOS tranistors and Paul K.Weiner, also from RCA, developped this idea employing a MOS with thin films of cadmium sulfide and cadmium selenide.

It is in 1960, when the integrated circuits with MOS begin to be produced in large scale, due to the discovery of the "planar" proceeding from FAIRCHILD. The first CI/MOS seems to be a work of Hofstein and Heiman from the RCA laboratories. This first integrated circuit was a network of eight transistors connected to perform the operation of a four inputs double gate. However, it should be necessary to wait for some years before all the parameters of fabrication could be controlled.

TRANSISTOR MOS.

1.2.2.1. Operation principles

In a typical MOS transistor, it is easy to find two islands of N type silicon, inside of a P type silicon substrate. The connections are made directly on the islands that receive the names of source and drain.



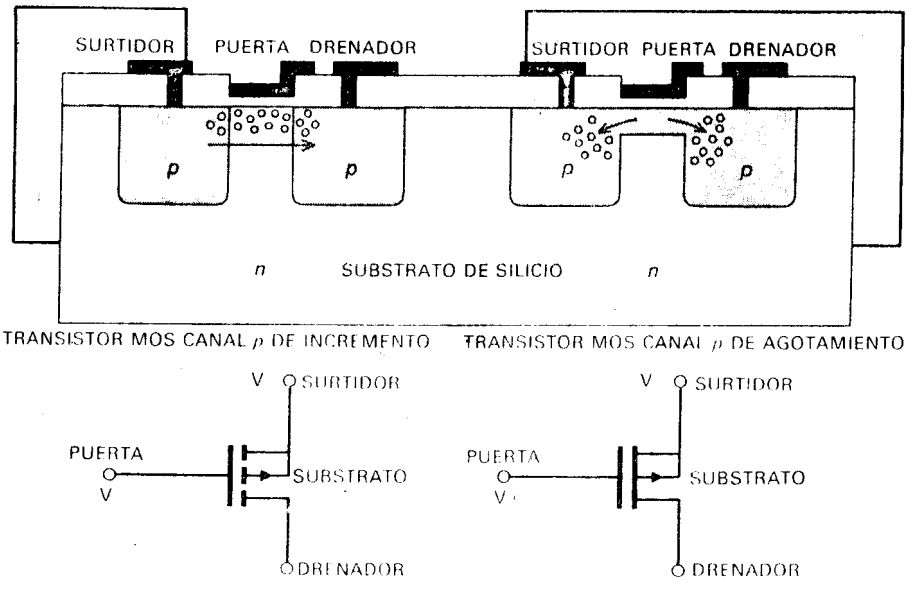
In the channel between source and drain, on the silicon surface, a film of silicon dioxide is deposited. On this dioxide film a metalic film is deposited, forming a new electrode whose name is gate. Silicon dioxide is a good isolator and we can say that the gate has no direct connection with the substrate. However, the gate is capacitively coupled to the substrate. Because of that the electric field generated by any charge that could be applied to the gate, will conditionate the mouvements of the carriers through the channel.

In normal operation, source and substrate are connected externally to a potential of 0 volts. Usually drain has a positive voltage. There is no current between source and substrate, as both are connected to ground. Between drain and substrate it will appear a small inverse current, just the same as occurs in the diode. When the transistor is in repose (i.e. without any voltage applied to the gate), the P type channel under the gate, has a lot of holes and the electrons that can be attracted to the positive potential of the drain are very few.

If we apply a positive voltage to the gate, the electrical field generated will attract many electrons to the thin cape placed in the surface of the crystal, under the gate electrode; Then due to the presence of many free electrons in a P region, we can say that the surface is inverted. This inversion generates between source and drain a continuous channel of N type. This continous channel permits the pass of a great current.

Until now we have described MOS operation only in the case when the conduction is due to electrons. Because of this electronical conduction this type of MOS device is called N channel MOS or simply MOSn.

The construction of the complementary device to the one we have described is possible. It will consist in two types P islands in a substrate N and with the same coupling of the gate electrode with the channel That is, capacitive coupling.
In this case all the polairities are inverses to the ones in the MOSn and the carriers that produce the current flow are the holes, in place of the electrons. Because of all that, this new MOS device is called MOSp.



Another type of MOS can be made by connecting two type N islands to a continuous N channel, placed under the gate capacitor. Because a continuous channel exists, when the gate is not excited (V_g = 0 Volts), the current can flow from source to drain. If we aplly a negative voltage to the gate, the electrical field generated will disable the current pass by taking out electrons from the channel. At this moment, we say that the transistor is cut. This type of MOS transistor receives the name of depletion MOS transistor. It is possible to fabricate the complementary device just changing the

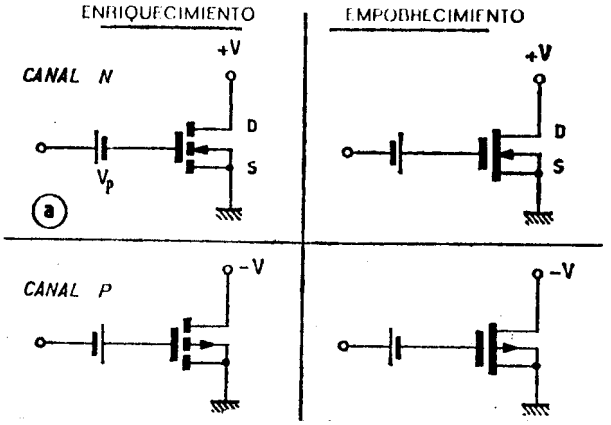
the semi-conductor types. In this case we will have a P channel.
Transistors that need a voltage applied to the gate in order to allow the conduction are called enhacement devices.
In brief, we can say that there are four different types of MOS transistors:

- N channel enhacement MOS
- N channel depletion MOS
- P channel enhacement MOS
- P channel depletion MOS

1.2.2.2. Symbols

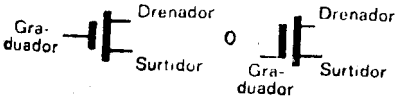
In order to avoid confusions, it has been decided to represent the MOS transistors of enhacement or depletion, N channel or P channel, as represented in fig. 2.1.
As the enhacement MOS does not permit the pass of the current in repose, we represent them with the channel interrupted.
As Depletion MOS conducts without command voltage, the channel is represented by a continuous line.

fig. 2.1.



However in practice, it is normal to use the same symbol for all MOS transistors, omitting the connection of the substrate.

fig. 2.2.



1.2.2.3. MOS fabrication

For the fabrication of a circuit with channel N enhacement MOS, it is used a silicon substrate of type N. In fig. 2.3. the different necessary operations are represented.

- Oxidation of the substrate surface. An oxide plate of 120. 10^{-3}microns of width is obtained.

- First operation of photogravure to create the source and drain zones.

- Creation of drain and source by diffusion of type P impurities.
- New oxidation of the obtained surface. A film of 1,4 microns is created.
- New photogravure operation to create the gate and the connections of source and drain.
- Elimination of the oxide film until the gate dielectric has a width of 0,1 or 0,2 microns.
- Last photogravure operation to liberate the zones that have to be analyzed.

The advantages of the fabrication of MOS transistors compared with the fabrication of Bipolar transistors are:

- It is not necessary to create isolation zones, that in the bipolar technology need the 30% of the substrate surface.
- It is not necessary the creation of epitaxial depo sits.
- It is only necessary a diffusion operation, while in bipolar technology the minimum necessary are four diffusion operations.

Fig.2.4. shows how MOS technology is simplet than bipolar technology by comparing two inverters.

fig. 2.3.

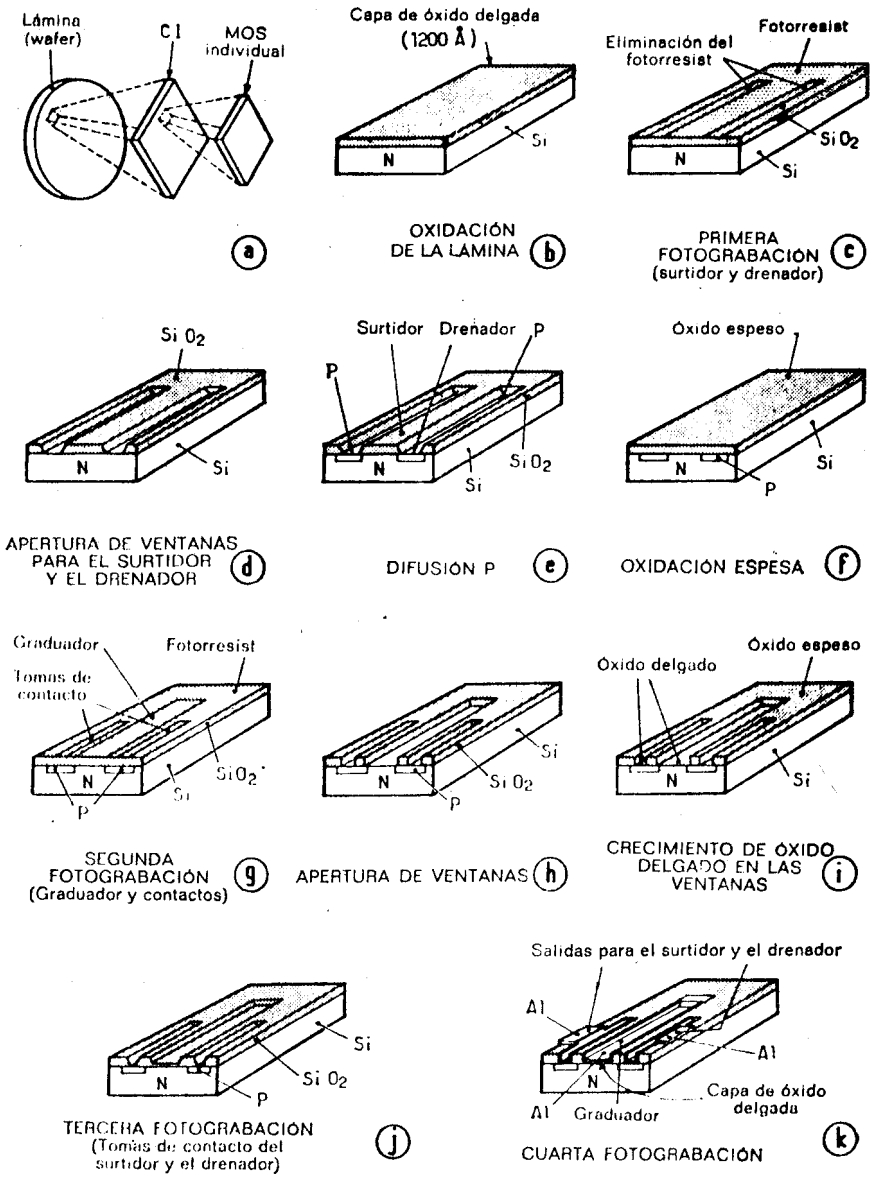
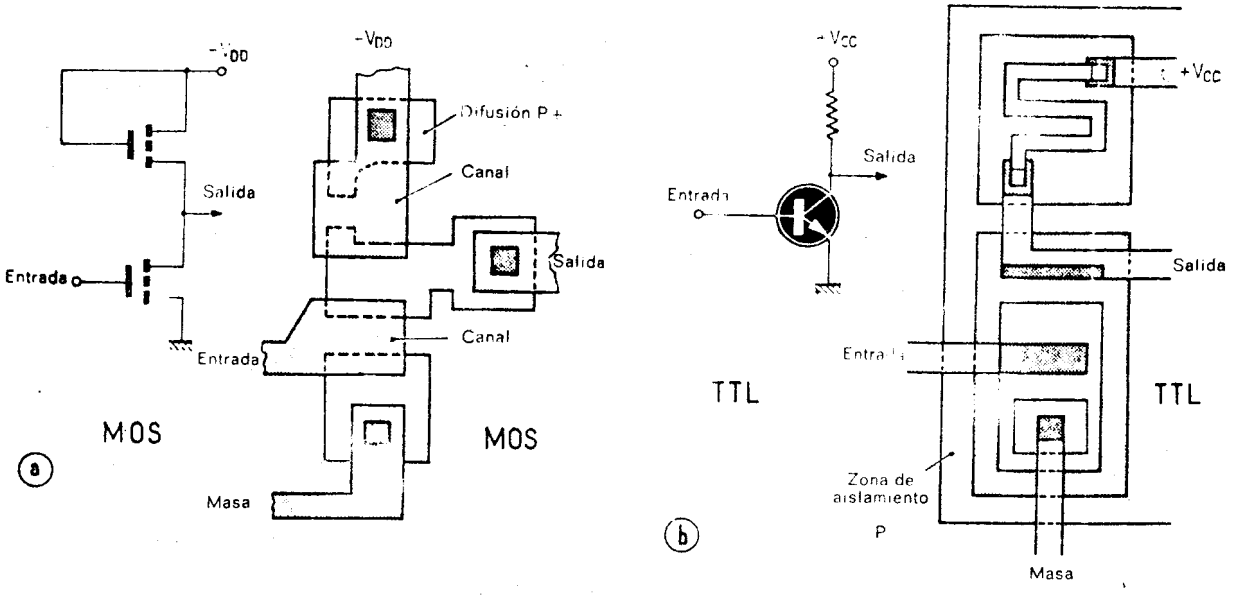


Lámina (wafer)
CI
MOS individual
a
Capa de óxido delgada (1200 Å)
Si
N
OXIDACIÓN DE LA LÁMINA b
Eliminación del fotorresist
Fotorresist
Si O2
PRIMERA FOTOGRABACIÓN (surtidor y drenador) c
Si O2
N
Si
APERTURA DE VENTANAS PARA EL SURTIDOR Y EL DRENADOR d
Surtidor
Drenador
P
DIFUSIÓN P e
Óxido espeso
OXIDACIÓN ESPESA f
Graduador
Fotorresist
Tomas de contacto
SEGUNDA FOTOGRABACIÓN (Graduador y contactos) g
APERTURA DE VENTANAS h
Óxido delgado
CRECIMIENTO DE ÓXIDO DELGADO EN LAS VENTANAS i
TERCERA FOTOGRABACIÓN (Tomas de contacto del surtidor y el drenador) j
Salidas para el surtidor y el drenador
Al
Capa de óxido delgada
Graduador
CUARTA FOTOGRABACIÓN k

fig. 2.4.

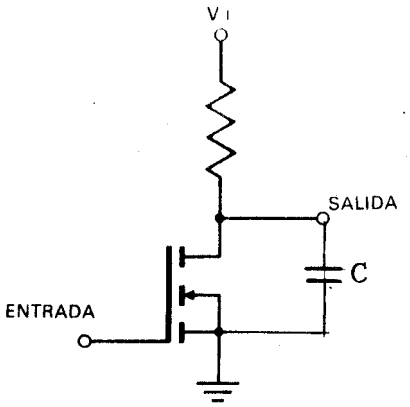

-VDD
Salida
Entrada
Difusión P+
Canal
Salida
Canal
Entrada
MOS
MOS
Masa
a
+Vcc
Salida
Entrada
TTL
+Vcc
Salida
Entrada
TTL
Zona de aislamiento
P
Masa
b

1.2.2.4. The MOS as a switch.

We are to study the MOS behaviour as a part of digital integrated circuits. These circuits use transistors as switches i.e. the transistors have to operate in cutoff or saturation.

Fig. 2.5. shows the first logical inverter used in MOS technology.

fig. 2.5.



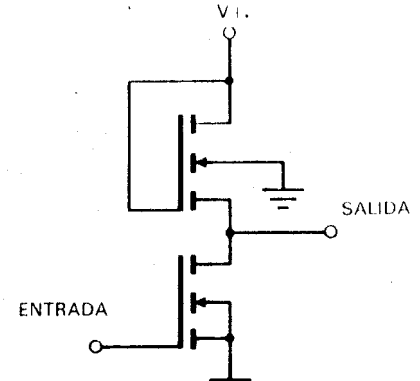
This inverter consistst in putting a load resistor to an enhacement MOS. When the input is high, the channel will be made. In this case, the transistor will become saturated and the output will have its lowest value. (logical "zero" = saturation voltage)
This circuit has three important disadvantages:

- it is difficult to integrate resistors
- when the output is zero, there is a high current consumption.
- the time constant when the output changes from 0 to 1 is different from the one of change from 1 to 0.

In a bipolar integrated circuit, the resistors are fabricated by diffusion methods and in a wafer it is only possible to obtain 200 ohms. That means that we need to connect 250 wafers in series, to get a resistor of 50 k. If we use a diffusion width of 10 microns, it will be necessary, for such a resistor, a length of 250 mm. and a minimum surface of 3 mm^2, which a an excessive value.

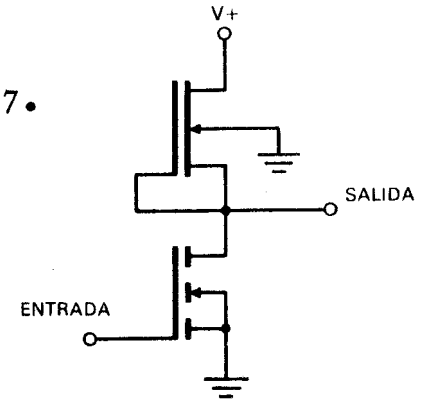
When dealing with MOS transistors, it is possible to use a transistor as load for another transistor, which will be the active one. The surface needed for a 50000 ohms resistor will be, using this method, 0,05 mm^2.
Then the resultant schem is shown in fig.2.6.

fig. 2.6.



With this method, theproblem of resistor integration is avoided.
The transistor used as load can be a depletion one, as shown in fig. 2.7.

fig. 2.7.

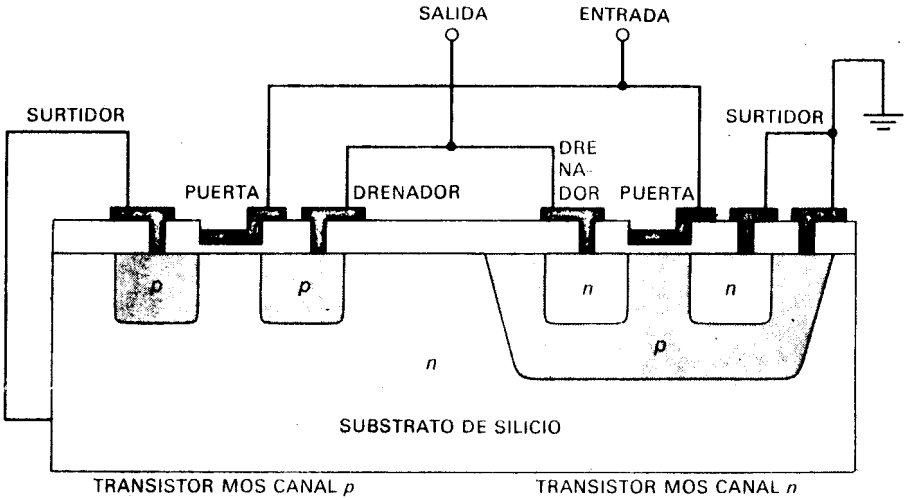


However the problem of high consumption and different time constants have not been solved.

1.2.2.5. The complementary MOS (CMOS).

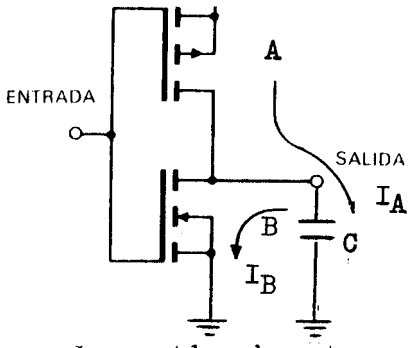
In order to solver the mentioned problems, RCA brought into the market in 1968 the first complementary MOS circuit family (CMOS), with the name of COS/MOS (Complementary Symetry MOS).
This family is based on the construction, in the same wafer, of two MOS transistors, an N type one and a P type one. If the circuit is fabricated in a N type substrate, as shown in fig. 2.8., it is possible to construct a P channel transistor. In order to construct the N channel transistor, it is necessary to diffuse before an N type island, which will serve also as separation of the two transistors.(It is a PN junction)

fig. 2.8.



The schematics of this device and the necessary connections are shown in fig. 2.9.

fig. 2.9.



In this figure we see that if we have the input connected to ground (logic zero), transistor A gets saturated, while transistor B is cut. In this situation, capacitor C, which represent the connection and associated logic capacities, will be charged to V+ voltage, due to the circulation of current I_A becomes 0.
If we connect now the input to the logical "one" (voltage V+), transistor A gets cut and transistor B through transistor B, by a current I_B. Once C has 0 volts, I_B is 0.
From this explanation, we can take two important consecuences:

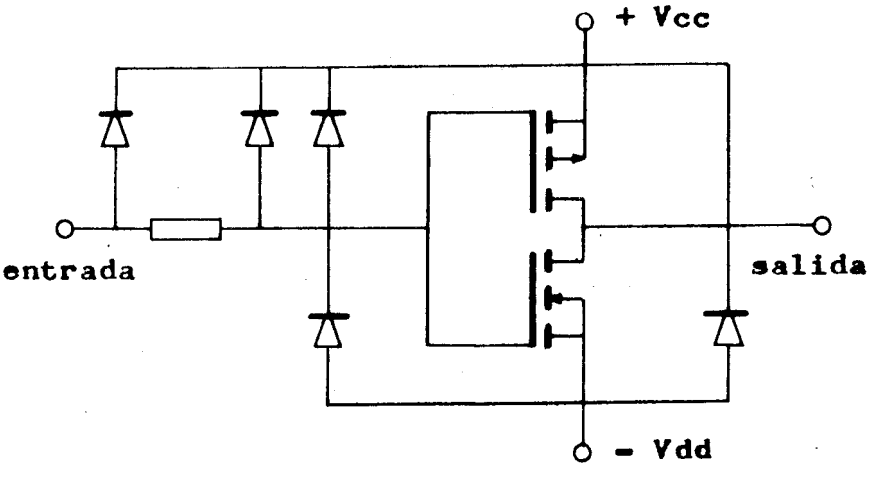
- There is only consumption during changes. This is very important, as the prior circuits has consumption while the output was 0.
- If transistors are fabricated completely symetric i.e. with the same electrical characteristics, the currents I_A and I_B are equal and this implies that the time constant for both changes are also equal

As a disadvantage, compared to the standard MOS families we can mention that the integration density is lower and that the complexity is higher.

1.2.3.0. MOS protections

The silicon oxide, that is used as dielectric, is 1000 Å wide and has a break voltage of 100 volts. A person that walks through a room with a waxed floor, generates, depending on the humidity of the ambient, from 4000 to 15000 volts. This means that if we touch with the fingers a pin of the chip, we can break the $Si\ O_2$, damaging the whole circuit.
In order to avoid this kind of accidents, MOS circuits have a protection network against excessive voltages. This protection network is composed by diodes as shown in fig. 3.1.

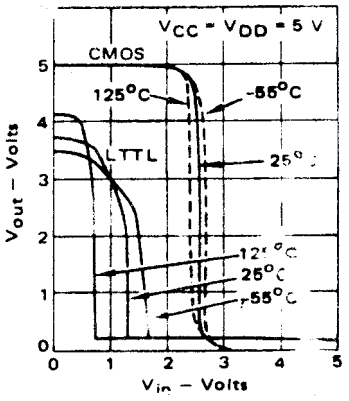
fig. 3.1.



1.2.4.0. Comparation of MOS and TTL families

Fig.4.1. shows the characteristic curves that relate: the input V_{in} with the output V_{out} of an inverter for the families CMOS and TTL.

fig. 4.1.



From the figure, we can take some conclusions:

- CMOS has better thermal stability than TTL
- The conmutation threshold is bigger in CMOS than in TTL. This has as a consecuence that CMOS has a better noise inmunity. (TTL has the treshold in 1,2 Volts, while CMOS has it in about a 45% of the supply voltage).
- The logic "one" is at 3,5 volts in TTL and V_{cc} in CMOS.
- The logic "zero" is at 0,5 volts in TTL and at 0 volts in CMOS.

Furthermore, as we have seen before, we could say that:

- The conmutation speed is smaller in CMOS than in TTL.
  The conmutation rate is: 8 to 10 Mhz for CMOS and 18 to 22 Mhz for TTL

This conclusion, that could be seen as an important problem, is not such a problem, as CMOS has the adequate speed to work with the rest of the technology employed with microcomputers, concretely in the case of PIN-BALL MACHINES.

- The CMOS can use a supply with voltages between 3 and 18 volts, while for TTL it has to be fixed to 5 Volts $\pm$25% and as it is obvious, really critical.
- CMOS has lower consumption than TTL has.
- As a disadvantage of MOS compared to TTL, we will say that CMOS is more expensive than TTL.

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3. What is a microprocessor?

1.3.0. Introduction.

A microprocessor is a logical device. More exactly an undefined variety of logical devices integrated in a unique chip.
The mictroprocessor is such an important device, that due to its existence most concepts of logical design have changed. Microprocessor logic is integrated in a chip, which is mounted in a Dual-In-Line package (DIP) We call logical device to the DIP and logical chip to the silicon wafer.
Microprocessors are very similar to big processors, but when comparing two microprocessors, the methods used to compare processors are not valid. What is used to compare processors, such as instructions sets, adressing modes and execution speed, have only a secondary role to the microprocessor user.
The important elements to compare microprocessors are:

a) The distribution in the chip of the logical devices that compose the microprocessor i.e. the microprocessor architecture.

b) The price.

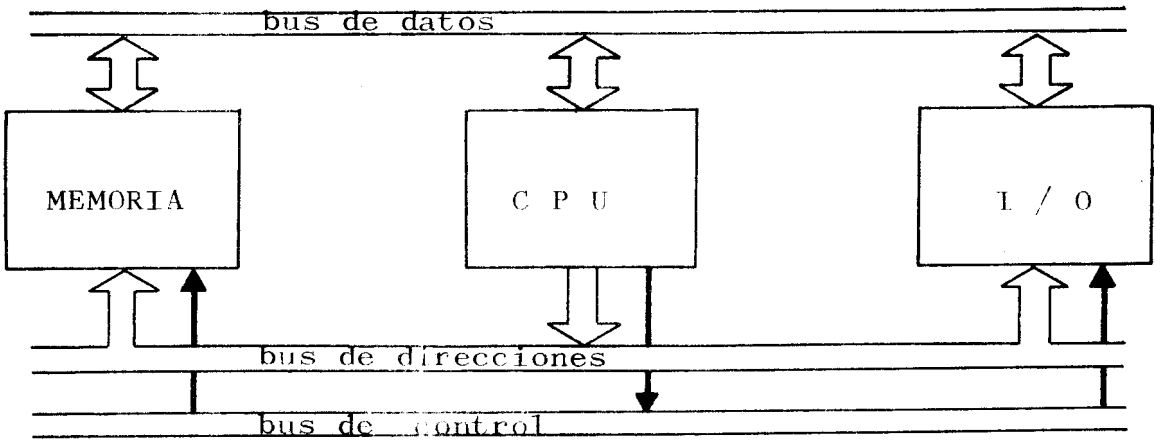
1.3.1. Historical evolution

The basic mathematical concepts for computer design were established in 1833 by Charles Babbage. With few differences, the actual computers are yet based in these concepts. In the twentieth century, the works of Von Neumann and N.Wiener contributed to the definitive developpement of computers.
In 1950 the UNIVAC I, the first computer, was constructed It was made of vacuum tubes and the place it needed, was a whole room. This kind of computers were very expensive and were only used in applications where the price was unimportant, such as resolution of mathematical problems, that could not be solved by other methods and military and spacial applications.
The advances in solid state phisics are the most important contributions to the increase of the speed of computers developpement.
Vacuum tubes were substituted by semiconductors, allowing the descent of the price and the opening of new markets by the ampliation of the possible applications of computers systems.
In 1960, the prices are so low that permit the use of computers in data processing.

In 1965, the PDP-8, from Digital Corporation, with a price of 50.000 dollars opens the field of computers to almost every potential user.
With this computer, the minicomputer age begins.
Today minicomputers can be bought for 1000 dollars.
These low prices, permit to the computers be more useful in more applications.
In 1969, Detapoint Corporation of San Antonio, Texas a company specialized in intelligent terminals and little systems with computers, together with Cogan and Viatron, tries to jump ahead and designs a very elemental computer. Afterwards makes a contract with Intel and Texas on the implementation of the mentioned design in alogical chip. Intel got it, but the execution of the instructions was ten times slower than the speed desired by Datapoint.
Datapoint refused this implementation and used discrete components. On the other side, Intel decided to sell the product and gave to it the name of Intel 8008. The microcomputers age had begun, and with it, a technological race.

1.3.2. Basic system of a microcomputer.

A microcomputer is a system able to make (input) store (memory), process (CPU) and deliver (output) information.
A basic system will be:



by some integrated circuits.
Let's analyze this scheme in more details:

1.3.2. (1) What is the bus?

Bus is a set of lines, that, connect, among them, all different blocks of the system. When a communication between a block and the bus is needed, the block becomes a low impedance state and receives or sends data to the bus.
When communication is not needed, the block becomes in a high impedance state, which is equivalent for the bus as if the block were disconnected.

In a microcomputer system, there are always three different bus types. The Data bus is composed by the lines that are used to transfer data. Usually there are the same number of lines as bits has the basic information processed by the microprocessor It is normal that the lines are eight.
The Address bus is composed by the lines that are used to indicate where data have to go. Usually it has sixteen lines. The Control bus is composed by the lines that the CPU uses to control the whole system.

1.3.2. (2) Memory block.
Memories are addressable devices used to store information. It consists in a group of bistable elements (each one of them stores a bit) and the necessary logic to indicate is the bistable elementwe want to write on or read from:
Generally, the microcomputers applications, consist in a set of integrated circuits.
We shall call volatil memories, to the memories that loss the stored information when disconnecting the power supply. On the contrary, a non volatil memory will conserve the information when disconnecting the power supply.

RAM memories (Random Access Memory). They are memories in which we can write or read. They are volatil.
ROM memories (Read Only memory) These memories can be read but not written. They are not volatil.
PROM memories (Programmable Read Only Memory). They are a special type of ROM's. They can be programmed by the user, but only once.
EPROM memories (Erasable Programmable Read Only Memory). They are PROM memories that can be erased. The erasure can not be performed for a single bit, it has to be a whole chip erasure.
EAROM memories. (Electrically Alterable Read Only Memory) They are similar to the EPROM's but they can be erased bit to bit, without erasing the whole chip.
Word Size of a computer system is the maximum number of bits that can be addressed by a single address. For example, if we deal with eight bit words, when we address a memory position, we are addressing eight bits. When dealing with microcomputers the word size varies among 4, 8, 12 and 16 bits, depending on the microprocessor type.
A set of eight bits is called BYTE. So, in a system with word size of 16 bits, each word will have two bytes. If the word size is eight bits, each word will be one byte. The set of 4 bits, is called NIBBLE.
The memory capacity is measured in K-words, K-bytes or K-birs, being $1K = 2^{10} = 1024$.

If we are told, that a system has a 2 KB memory we will know without ambiguity, that the memory has 2 K bytes, but if we are told, that the memory has 2 KW, we should ask for the word size, to know which is the memory capacity.

When we want to access to a memory position, we give to the address bus a set of 16 bits, that correspond to the desired position. From these bits, a first group will select a chip and the others will select the position in the chip.
For example, if we use a 65 KW memory, implemented with 65 chips of 1KW capacity each chip, we will use 6 bits to select the chip corresponding to the desired position and the other 10 to select one of the 1024 words of the chip. That is, the minimum length of the addressing will be 16 bits.
For example: If we want to access to the address 1DAE, we will have:

Total address = 0001 1101 1010 1110 = 1DAE

chip select= Ø7 internal address = 1AE

and we will select the position 1AE of chip Ø7.

The contents of a memory position can be interpreted in different manners:

a) As a numerical data in binary form.
b) As a coded data
c) As a part of a data that needs more than one memory position.
d) As an instruction code.

This implies that the microprocessor must know in every moment what is being read from memory.

1.3.2. (3) Central processing unit (CPU) block

The logic that compose the central processor unit of a microcomputer is implemented in a single chip, which receives the name of microprocessor. (uP).
This logic changes very much from a microprocessor to another, but all of them have some fundamental necessities to satisfy.
Basically they must have:

a) A set of registers.
b) An arithmetical-Logic unit
c) A control unit
d) Some indicators of the microprocessor state (status flag)
e) A clock

There will be four classes of registers:

1) Acumulator
2) Data counter
3) Instruction register
4) Programm counter

The CPU will have one or some registers to store the data that have been read from the memory. These registers will have the same numbers of bits as the used words. Usually they have 8 bits. These registers receive the name of acumulators. Normally the CPU operates on the contents of the acumulators.
The data counter is a register, which stores the address of the memory position in which it is necessary to read or to write. This register will have the same length as the address words. Usually this length is 16 bits.
The instruction register, is used to store the code of the instruction that has to be executed. Has the same length as the words. Usually 8 bits.
The program counter, contains the address of the next instruction that has to be executed, in order to allow the microprocessor the operation of lecture from memory. The length will be the same as the address words, i.e. 16 bits.

The ALU (Arithmetic and Logic Unit), has to be able to perform the following types of operations:

1) Binary addition
2) Boolean operations
3) Word complementation
4) Shift a word to the right or to the left.

The control unit is engaged with the decoding of the instruction that have to be executed and with the control of the logical elements of the ALU, in order to perform the desired operations.

The status flags are a set of bits that are set to 0 or to 1, depending on the results of the operations in the ALU. The operation of the status flags are completely automatic.
The typical significations of the flags are:
Zero, Carry, Sign, Overflow, Parity and Intermediate carry.
The operations inside of the CPU are controlled by a clock. This clock is usually controlled by a cristal and the period is between 100 nsec and 1 usec. From this basic clock, all control signals of the system are constructed.

1.3.2. (4) Input output block (I/O)

The input output operations are transferences of data between the microcomputer system and the external logic. There are many different ways to perform these transferences. But it is usual to clasify them in one of the following types:

1) Programmed
2) Through interrupts
3) DMA, direct to memory access

Programmed I/O transferences are the transferences between the system and the external logic, that are completely controlled by the program that is executed by the CPU. In order to allow the correct funcioning of this type of I/O operations, it is necessaty to have a well defined protocol wose mission will consist in indicating to the external logic tjat a data is ready to go out (output operations) and indicating to the microcomputer that an external data is ready to be read. As we mentioned before, all this transfer operations are performed through ports. So, the protocol will be able to recognize if an external data has been collocated in an input port and to excite the external logicm in order to indicate that an internal data has been collocated in an output port, allowing the transfer operation.

The input and output operations that are controlled by interrupts receive the name of interrupt inputs or interrupt outputs. The secuence of operations performed while executing an interrupt I/O is the following:

The CPU receives the interrupt signal from the external logic. The CPU ends the execution of the instruction that was executing and sends to the external logic a signal to indicate that the interrupt signal has been received. At this moment, the CPU analizes the vector interrupt, which informates the class of interrupt and the address that has to be put in the program counter. This address corresponds to a service routine, which performs the I/O operation. When this routine is finished, the program, that was being executed when the interrupt signal was received, continues.

All this secuence can be more complicated if the microporcessor has interrupt priorities.

The DMA I/O operations are I/O operations which are performed between the memory and the external logic without the control of the CPU.

4. The microprocessor COSMAC CDP 1802

1.4.0. Introduction.

This microprocessor has been designed to give to the user a powerful logical device more than to perform complex programs. It has been fabricated in MOS technology. The fact of being fabricate in CMOS technology provide us a lower power consumprion with a single power supply and a great noise protection.
The power supply can change its voltage between 3 and 12 volts and the temperature range is from -55ºC to ± 125ºC
The companies that fabricate this microprocessor are RCA (the most important production) and Hughes Aircraft Inc.

1.4.1. Architecture

As it

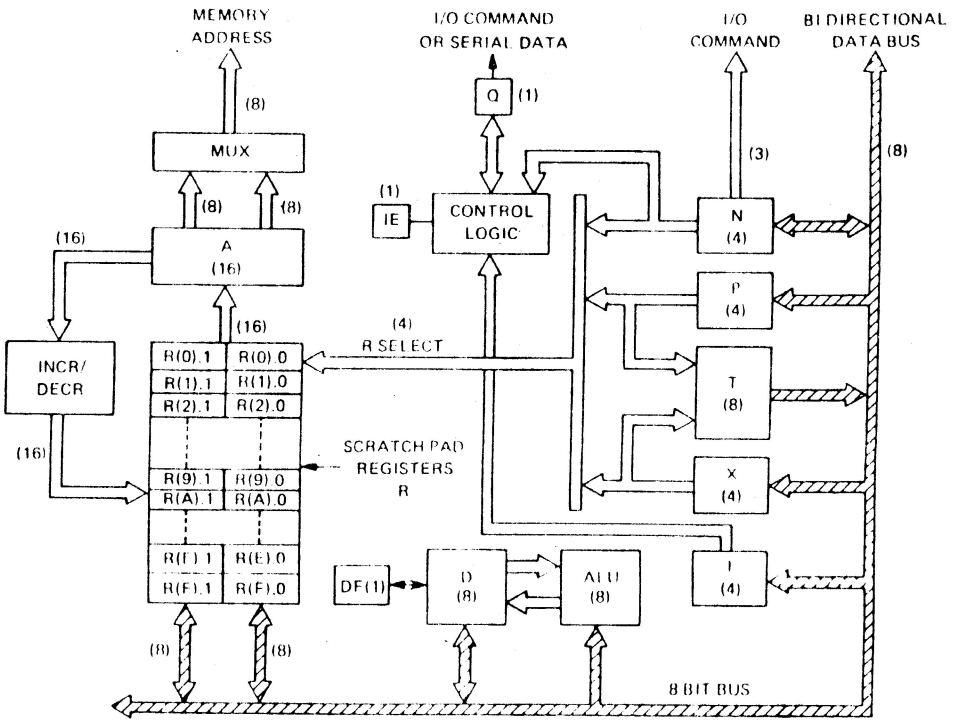


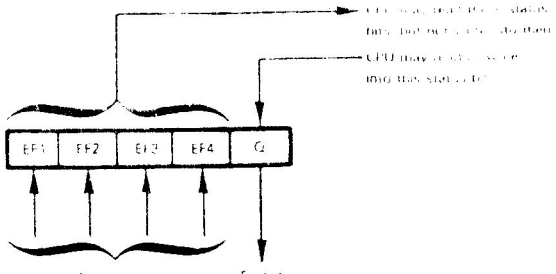
Fig. 2 – Internal structure of the CDP 1802 Microprocessor.

As it is easy to see in the figure, this microprocessor has 16 registers of 16 bits, which are called R(0); R(1), ... R(F). These registers can be addressed as 16 bits registers and as 8 bits registers, by addressing the higher or lower byte. When dealing with the registers bytes their names will be R(0).1 and R(0).0 for the higher and the lower bytes of the R(0) respectively.

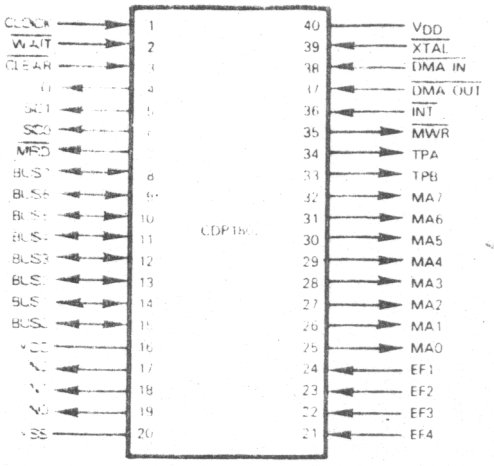
All these registers can be used as program counter or data counter.
In order to indicate which is the register that has the function of program counter, we have a 4 bits register called P register and to indicate which is the register with the function of sata counter another 4 bit register the X, is used. The contents of all these registers can be modified by the program.
The register T, is an 8 bit register which is used to store the contents of X and P, when it is desired to change them but keeping their value. As an example of its functioning, we have the interrupt secuences, in which the values of PC and DC have to be kept.
Registers I and N, are four bits registers and together can be seen as an instruction register, as the higher 4 bits of the instruction code are stored in the I register and the 4 lower are stored in N.
The D register has 8 bits and is used as acumulator. When we use the R registers type as a RAM memory, all data transferences have to pass through D registers.
DF is a 1 bit register and is used as carry flag.
IE is a 1 bit register that can be modified by program and whose function is to accept or to deny the access of interrupts to the CPU.
Q is a 1 bit register, that can be modified by program and serves as status flag and output.
Register A, is a 16 bit register and is used to change the 16 bit addresses to 8 bits words. The reason of the existence of this register is that the COSMAC buses are 8 bits buses. From the R type registers, the R(0) is used for the DMA's R(1)is used to indicate where the service routine begins and R(2) is used to indicate the memory position from which T register has to be loaded or to which the contents of the T register has to be sent. That is, R(2) is used as a promitive stack pointer.

1.4.2. Status flags

This microprocessor provides seven stat indicators. One of them is the data fkag, which is equivalent to the carry status and is located in register DF. This indicator tell us if we have a carry in the most important bit, when performing an addition.
Another flag is the Interrupt enable flag, which is register IE, already mentioned. Another is the Q status, already studied.
There are four other flags, that are connected to the microprocessor pins and that are set to 0 or to 1 by the external logic. The names of these registers are: EF1, EF2, EF3, and EF4. The CPU can check all these flags by program and take decisions, depending on the value os the status flags.



1.4.3. Pins and signals



Pin Name	Description	Type
BUS0 - BUS7	Parallel Data Bus	Bidirectional
MA0 - MA7	Address Bus	Output
CLOCK	Externally generated clock	Input
XTAL	External crystal connection	Input
TPA, TPB	Timing pulses	Output
EF1 - EF4	External flags	Input
Q	Q status	Output
SC0, SC1	State Code lines	Output
MWR	Write pulse	Output
MRD	Read level	Output
N0 - N2	I/O command	Output
WAIT, CLEAR	Control lines	Input
DMA-IN, DMA-OUT	Direct memory access control	Input
INT	Interrupt request	Input
VDD	Internal voltage supply	
VCC	Input/Output voltage supply, logic 1	
VSS	Ground, logic 0	

Figure 11-2. CDP1802 COSMAC CPU Signals And Pin Assignments

Thereare 16 bus lines.

BUS Ø - BUS 7.- It is a typical bidirectional data bus; that is, the information can go in and out through the same place. All data fo in and out through these lines.

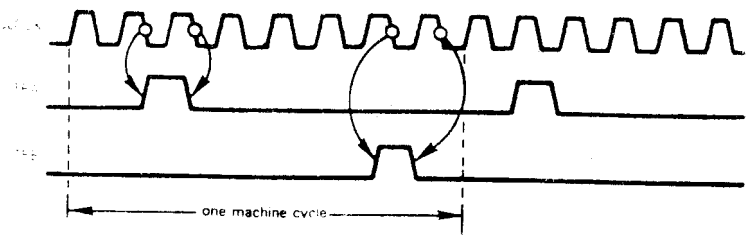
MA Ø - MA 7.- It is an address bus of 8 bits. As all the addresses are of 16 bits, all accesses to memory have to be multiplexed, i.e. the 8 higher bits are transferred first and then the other 8. This is, of course, a problem, because it will force to use a more complex interface for the memory, but furthermore, is a great advantage as we will have 6 free pins that can be used to take of give some control signals from or to the external logic.

There are also four temporization lines:

CLOCK.- Input to the CPU of the external clock signal. It is the main temporization signal and can reach 6,4 Mhz when the voltage supply is 10 volts.

$\overline{\text{XTAL}}$.- This line is used when the chip internal clock is used. Then, an external crystal with a paralell resistor can be connected between XTAL and CLOCK

TPA and TPB.-They are temporization pulses, that indicate the beginning and the end of a machine cycle respectively, as shown in the figure. A machine cycle is composed of 8 clock signal periods.



There are 7 status lines:

EF-1 EF4 already explained.

Q already explained

SC Ø - SC1 They are two outputs that are used by the CPU to indicate which is the machine cycle that is being executed. The truth table is:

SC1	SCØ	MACHINE CYCLE TYPE
0	0	Instruction seek and decoding (fetch)
0	1	Instruction execution
1	0	D.M.A.
1	1	Interrupt examination

There are 10 control lines:

$\overline{\text{MWR}}$.- When is 0 indicates an access to memory operation. This line becomes 0, when the lower order byte of an address is stabilized in the address bus.

$\overline{\text{MRD}}$.- When is 0, indicates that the CPU is reading data from memory or from an input port. When is 1 indicates that the CPU is sebding data to memory or to an output port.

NØ - N1 - N2.- These three lines are 0 when no I/O operation is performed, at least one of these lines bcomes 1.

$\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$.- They are two inputs that force the CPU to one of the following states:

CLEAR	WAIT	CPU STATE
0	0	LOAD
0	1	RESET
1	0	PAUSE
1	1	RUN

During the load state, the external logic can perform DMA's. In the reset state, registers I,X,P,R,(0) and status Q becomes 0.
In the state Pause, all the internal operations of the CPU are stopped, except the clock signal.
The run state is the normal operation of the CPU.

DMA-IN and DMA-OUT.- They are control signals that come from the external logic and order DMA operations.

INT.- It is an external control singal that comes from the external logic. When this signal is 0, an interrupt is required.
There are also three supply lines.

V_{DD}.- Provides the internal supply voltage.

V_{CC}.- Provides the CPU inputs and outputs supply voltage and gives information about the voltage of the logical level 1

V_{SS}.- Provides ground and gives information of the voltage of the logic level 0.
So the CPU chip has 40 pins.

ELECTRICAL DATA

e following pages contain specific electrical and timing characteristics of the COSMAC P1802.

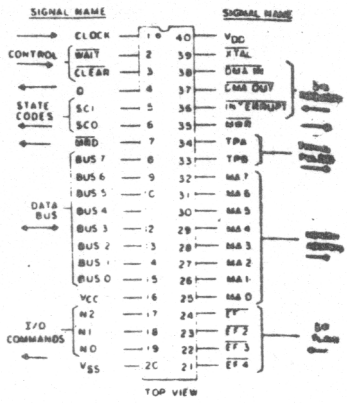
Preliminary CDP1802D, CDP1802CD

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC			CONDITIONS V_O (V)	CONDITIONS V_{CC}, V_{DD} (V)	CDP1802D TYPICAL VALUES	CDP1802CD TYPICAL VALUES	UNITS
uiescent Device Current, I_L			–	5, 5	100	500	µA
			–	10, 10	500	–	
			–	15, 15	1000	–	
tal Power Dissipation; P CODE "00" See Fig. 4)	f = MHz	3.2	–	5, 5	6	8	mW
		5.0		5, 10	30	–	
		6.4	–	10, 10	40	–	
utput Voltage Low-Level, V_{OL}			–	5, 5	0.01	0.01	V
			–	10, 10	0.01	–	
High-Level, V_{OH}			–	5, 5	5	5	
			–	10, 10	10	–	
oise immunity nputs Low, V_{NL}			0.5	5, 5	2.25	2.25	V
			–1	10, 10	3.45	–	
nputs High, V_{NH}			4.5	5, 5	2.25	2.25	
			9	10, 10	3.45	–	
utput Drive Current N-Channel (Sink), I_{DN}			0.4	5, 5	1.5	1.5	mA
			0.5	10, 10	3.0	–	
P-Channel (Source), I_{DP}			2.5	5, 5	–1.6	–1.6	
			4.6	5, 5	-0.4	-0.4	
			9.5	10, 10	-0.9		
nput Leakage Current Any Input), I_{IL}, I_{IH}			–	5, 5	±1	±1	µA
			–	15, 15	±1	–	

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg})
. . . . . −65 to +150°C
Operating-Temperature Range (T_A)
. . . . . −55 to +125°C
DC Supply-Voltage Range (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
$V_{CC} \leq V_{DD}$
CDP1802D . . . . . −0.5 to +15 V
CDP1802CD . . . . . −0.5 to +7 V
Power Dissipation Per Package (P_D)
For T_A = −55 to +100°C
. . . . . 500 mW
For T_A = +100 to +125°C
. . . . . Derate Linearly to 200 mW
Device Dissipation Per Output Transistor
For T_A = −55°C to +125°C . . . . . 100 mW
Input Voltage Range, All Inputs
. . . . . −0.5 to V_{DD} +0.5 V
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 s max: . . . . . +265°C

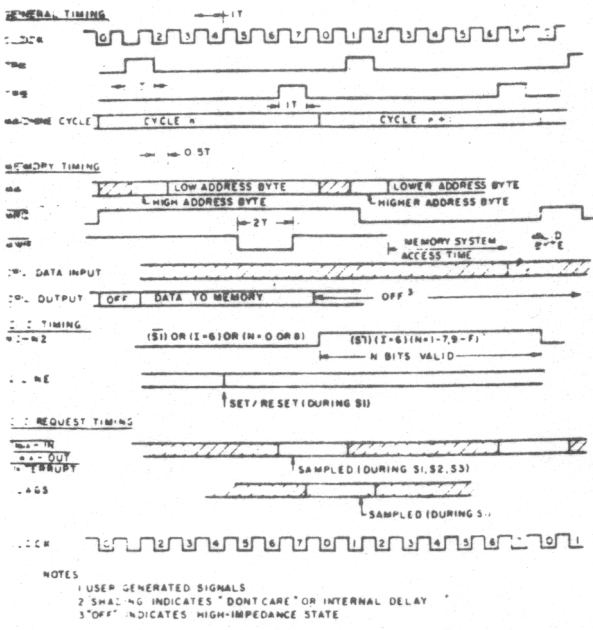


Terminal Assignment for CDP1802

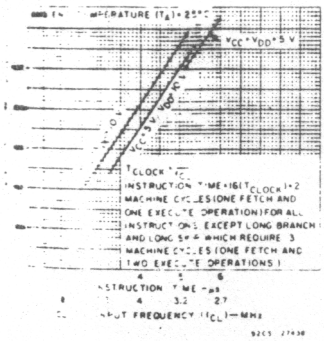
OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES		UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802D	CDP1802CD	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	–	–	3 to 12	4 to 6	V
Recommended Input Voltage Range	–	–	V_{SS} to V_{CC}	V_{SS} to V_{CC}	V
Clock Input Rise or Fall Time, t_r or t_f	3-15	3-15	5	5	μs
Instruction Time[2] (See Fig. 3)	5	5	5	5	μs
	5	10	3.2	–	
	10	10	2.5	–	
DMA Transfer Rate	5	5	400	400	KBytes/s
	5	10	625	–	
	10	10	800	–	
Clock Input Frequency, f_{CL}	5	5	DC - 3.2	DC - 3.2	MHz
	5	10	DC - 5.0	–	
	10	10	DC - 6.4	–	
Clock Pulse Width, t_{WL}, t_{WH}	5	5	160	160	ns
	5	10	100	–	
	10	10	80	–	
Clear Pulse Width	5	5	300	300	ns
	5	10	200	–	
	10	10	150	–	

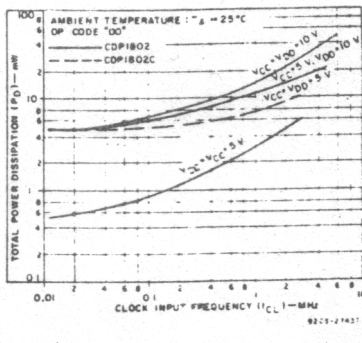
Notes:
1. $V_{CC} \leq V_{DD}$; for CDP1802CD $V_{DD} = V_{CC} = 5$ volts.
2. Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.



Timing diagram.



Typical instruction time vs. memory system access time.



Typical total power dissipation vs. clock input frequency.

4. General structure of the machine

The machine has an information recollector unit, which is controlled by the MPU. This unit has the structure of a contacts matrix. The information recollected, is processed by the CPU. The CPU performs this process by executing the program stored in two ROM memories. As results, it takes information out of the MPU through the output unit. This output unit has also the structure of a contacts matrix. The information that comes from the first column (a,b,c,d,e,f,g, OL and LP) together with the signals of match and game control, supply (±) and ground (N), goes to the MATCH-GAME plate. Information coming from the second and third columns (N1,...N8 and D1,...D4 respectively) is sent to the DECODER plate, The function of the DECODER plate is decoding all this information and distributing it to the corresponding plates. The plates that are dependent from the DECODER are:

The four players DISPLAY plates

The relay plates except the Z relay that is directly controlled bu the MPU.

thc sound plate

and, in the Spce Gambler machine, also the cone lights plate.

In the DECODER plate, there are also the thyristors, that control the bumper and the four players lamps. In this plate is also the LED corresponding to the test point and supply for the plates, that the Decoder controls, for the bumper lights, for the cone and for the player in play light.

The informationfrom the 4th, 5th and 6th columns (U1, ... U8; V1,....V8 and W1,...W8 respectively) of the MPU output matrix is sent to the thyristors plate that controls the same lights.

All electronic part and game lights take their supply from outputs 10Va. Ov. 10Vb of the supply transformer. The fixed lightd, take their supply from outputs 0-7V of the transformer.

The inductor part, takes its supply from outputs 0, 28V, 30V and 32V. The inductors set is divided in two groups, one of them uses DC supply and the other one, uses AC supply. The AC group is composed by the four inductors that control the movil targets (Space Gambler) A.B.C.D. and the inductor of the Ball-taker. These inductors are connected in series and are controlled by tge SC relay. The AC group is also composed by the TACA inductor, which is controlled by the ZB relay. In the machine BIG TOWN, there is a separated relay to control the lifting of the target batteries, whose inductors are series connected and supplied with 110 volts by a rectifier.

The DC group is composed by the two bumper inductors, the ball-hitters and the flippers. All these inductors are controlled by the game relay Z. This relay connects the inductors when the machine is in play or in TEST positions and disconnects them, when the machine is in GAME OVER. In the machine BIG TOWN, the Z relay has an inverter to take the ball from the hole (HOLE KICKER).

5.- Relays plate

The scheme of the plate shows that there are four relays controlled by four transistors. The relays supply is the 10 volts lines (+) and (-), that come from the decoder module.

In this plate, transistors are used as switches. The control inputs are TR (not used in Spce Gambler and Big Town), ZB, used to control the TACA relay, SC used for the Ball-Taker relay, and Z for the game relay. When the control input is high (logic 1), i.e. 10 volts, the transistor conducts and the relay gets closed. When the control input is lowm the transistor is open and the relay keeps open. The function of the relay is connecting the OV line of the inductors supply to terminals OC, SD, TC and TP. (see wiring and relays board schematics)

6.- Cone lights plate

(Only Space Gambler)

As it is easy to see from the plate schematics, there are three control inputs: CO 1, CO 2, and CO 3 and two supply inputs (+) and (-), which are 10 Volts lines. Everything comes from the Decoder plate. The three control signals can be 0 or 1 (i.e. 0 or 10 volts) and are decoded by the integrated circuit 4028 to know which of the six stages has to get lighted. For example, if CO1 = 1, CO2 = 0 and CO3 = 0, using the truth table of IC 4028 we will see that all outputs will be 0 except nº 1, which will be 1.

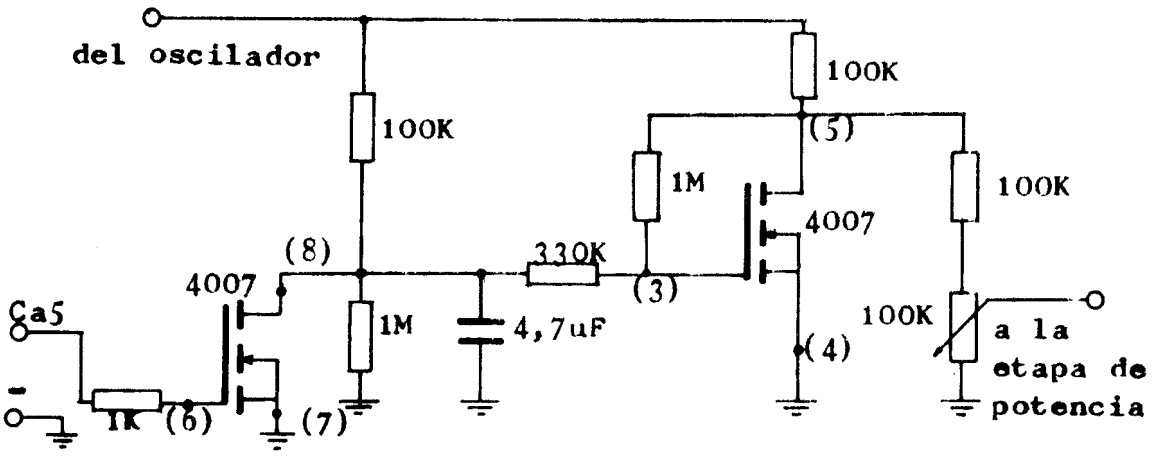
These outputs are connected to the thyristors gates which are series connected with the cone lights stages. When we have 1 at the thyristor gate, the thyristor will not conduct and the lights of stage 1 will be on and the rest of the stages will have their lights off (see wiring and plate schematics).

7.- Sound plate

There are 5 control inputs (ca 1, ca 2, ca 3, ca 4, ca 5 and two supply inputs (+) and (-). The supply voltage is 10 volts. Everything comes form the DECODER plate.

The oscillator is implemented with three inverters of the 4069 intergrated circuit, two resistors of 10K and a capacitor of 1Kpf. The integrated circuit 4016 has 4 CMOS switches. The control signals to these switches are Ca 1, Ca 2, Ca 3, and Ca 4. When Ca 4 is 1 and Ca 1, Ca 2 and Ca 3 are 0, the oscillating circuit closes through a 240 K resistor, that is between ourput 2 and input 1 of the integrated circuit. Then, the oscillator has a frequency of 988 Hz, which is the frequency of the 100.000 points note.

By changing the resistor, through which the oscillator circuit closes, the oscillating frequency can be changed. As we have four different switches, we will have four different note. Integrated circuit nº 4016 has a functio function of interface between the digital part, which comes from the DECODER and the analogical part, that goes to the loudspeajer. Intefrated circuit 4007 is composed of two complementary pair of transistors with inverter, but, in fact only the two transistors used as variable resistors are used. The circuit is as follows:



From the oscillator comes a square wave whose range is from 0 to 10 volts. When Ca5 is 1, the transistor between pins 6,7 and 8 of the integrated circuit 4007, conducts and the 4,7 uF capacitor can not be charged. This forces the transistor between pins 3,4 and 5 of IC 4007 to remain in cutoff region and the whole signal coming from the oscillator goes to the power section producing a constant volume note.
When Ca 5 is 0, the first transistor is cut, forcing the signal that comes from the oscillator to charge the 4,7 uF capacitor. As this capacitor is getting charged, the second transistor begins to conduct and takes current untol the capacitor is completely charged from the signal that comes from the oscillator. At this moment the second transistor is saturated and the whole signal is derived to ground through the transistor. So, no part of the signal goes to the output section and the sound is stopped.
The fading of the sound is performed with this method.

8.- Displays plate.

Looking to the schematics of the four displays plates, we see that they have a 10 volts supply (+), ground and signals L1.....L8 all in parallel. Furhtermore, the 1st player plate has three control lines: 100000-10000 1000-100, 10-1 and the other three plates, only two control lones: 100.000-10000 and 1000-100. All these lines come from the DECODER.

From the eight lines that have the information of the number to be displayed, four lines go to the displays of 10000, 100 and 1 (L1, L2, L3 and L4) and the other four lines fo to the displays of 100.000, 1000 and 10 (L5, L6, L7, L8). Note that it is only necessary four bits to decode a digit.

When the three control signals are 1, IC 4511 do not allow the pass of the information contained in (L1 ... L8). When one of the control signals is 0, the information contained in L1 ....L8 is sent to the displays pair controlled by the signal. The other displays are unaffected

9.- Match-Game plate

The scheme of this display, is included in the schematics of the MPU plate. All signals and supply come from the MPU. The supply inputs are (+) 10 volts rectified and N (ground), There are two signals (1P and 01), that force, when have value 1, the 1 of the games and the two zeros of the lottery (match) respectively. This operations are performed by switching the transistors shown in the schematics. There are secen signals A,B,C,D,E,F and G, which are in parallel with the game and match digits. Control signals L and P indicate the digit to which the information corresponds.

The real operation is as follows:

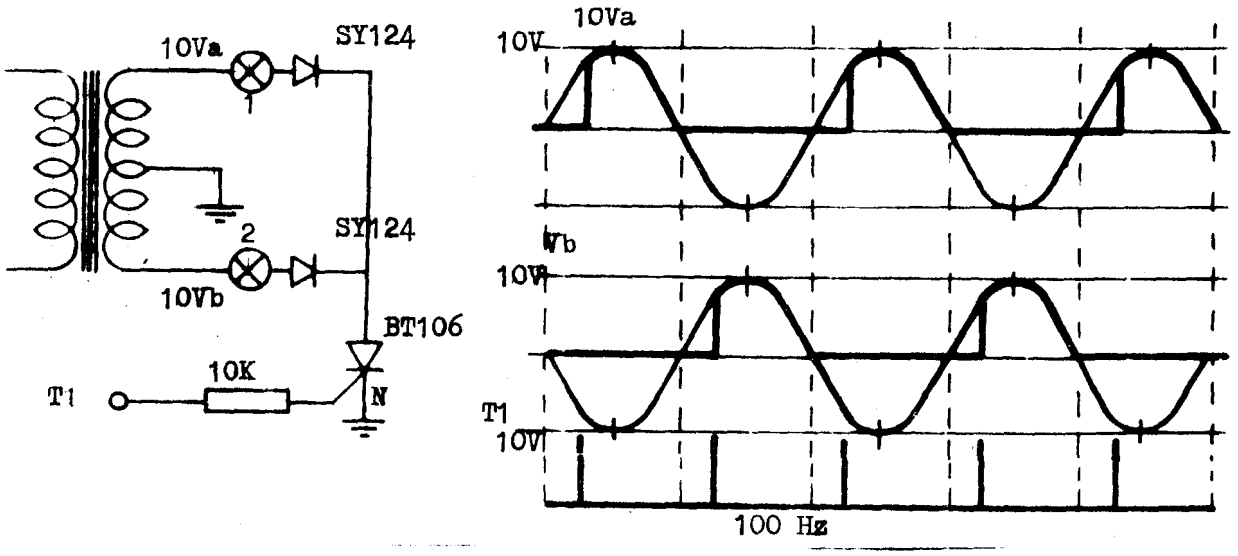
We turn on a digit and turn off another at a speed of 50 Hz. At such a switching rate, the human eye sees the digit continously lighted.

10.- Thyristor plate

Outputs V1 ....V8; U1 .....U8; W1.....W8 of the MPU go directly to the thyristor plate. There is an equivalence sheet to know the names of the signals in the MPU plate and their corresponding names in the thyristors plate, T1....T24.

Each thyristor controlls two lamps, as shown in the schematics. The cathodes of the 24 thyristors have a common ground, that is the intermediate terminal of the transformer. 24 lamps have aldo a common supply, which is a 10V connector of the transformer and the other 24 lamps have as common supply the other 10 V connector.

The operation is as follows:
When TL is 0, the thyristor is cut and no lamp is lighted. When T1 receives a 1, the thyristor conducts and the lamp, to which the 10 Volts half wave is positive, gets lighted, remaining the transistor in its conduction state until the q0 volts half wave becomes 0.
It is at this moment when the thyristor gets cut.
The CPU knows in every moment, which is the corresponding half cycle. So, depending on the half cycle of the moment, the CPU sends information to the thyristors to light the lamps corresponding to that half cycle. For example, if we want to turn on the Tilt lamp (nº 1) and turn off the fourth die lamp (nº 2)m we must send 1 during the half cycles with positive Va and 0 during the half cycles with with positive Vb.
The signal will be a pulse train of 50 Hz. If we wanted ti light both lamps, we should send a 1 in both cases. That would produce a 100 Hz pulse train.



11.- Decoder plate
This plate has twelve inputs coming from the MPU; (N1....N8 and D1....D4) and three supply inputs (Q, R, N). This supply inputs are: the two 10 volts connections and the intermediate terminal of the transformer (10Va-0-10Vb)
The power supply, made with transistors MC 140 and TIP 33 is used for decoder, displays, sound, relays and cone (if exists) plates.
The rectified output (+L) is used to supply the bumpers, players and cone lamps.
From the twelve inputs, eight (N1....N8) have information and four (D1....D4) bring the code that indicates to what corresponds the information.
IC 74C42 is a binary to decimal decoder, that puts a 0 at the selected output, mantaining in the rest of the outputs to 1.

We need 11 outputs and IC74C42 provides only ten. So, we must use the IC 4023 to implement completely the decoder. Output 0 of the IC 74C42 is connected to the clock of IC's nº 7 and that are 74C175 latches. Output 1 is connected to circuits 5 and 6. The rest of the outputs control the players displays.
The pass of information from inputs to outputs occurs when there is a transistion from 0 to 1 at the clock of latches 74C175.
IC's nº 1, 2 and 3 are LM324 operational amplifiers, which are used when the MPU uses EPROM memories. Their mision is to amplify the logic level 1 from the 5 volts that has in the MPU plate, to the 10 volts that is the voltage used in the rest of the machine. If the MPU uses ROM memories, this op.amp. are not necessary because the voltage of the logic level 1 in the MPU plate, is ten volts in this case.
When these operational amplifiers have at the input a voltage higher than the voltage reference of 2,7 volts, which is at the voltage divider of 22K and 10K, at the output apprears the supply voltage which is: 10 volts. If at the imput we have a voltage lower than 2,7 volts, the output will be 0 volts.
These operational amplifiers operate saturation regime i.e. as switches (more correctly as schmidt triggers, but without hysteresis cycle). This kind of operation is performed by the resistor of 220 K, that operated as a positive feedback.
This type of operation permits that if at the input we have 10 volts, at the output we will have 10 volts too. Because of that,we see that decoders for EPROM are valid also for ROM but not vice-versa.

The truth table is as follows:

D_1	D_2	D_3	D_4	0 = 74C42 output low	CONTROL
0	1	0	1	output 10 of 4023	Player display 4, 1000-100
1	0	0	1	11	J4. 100000 - 10000
0	0	0	1	10	J3. 1000 -100
1	1	1	0	9	J3. 100000 - 10000
0	1	1	0	7	J2. 1000 - 100
1	0	1	0	6	J2. 100000 - 10000
1	1	0	0	5	J1. 10 - 1
1	1	0	0	4	J1. 1000 - 100
0	1	0	0	3	J1. 100000 - 10000

In all these cases N1.....N8 go directly to the displays selected by the control.

The rest of the controls are:

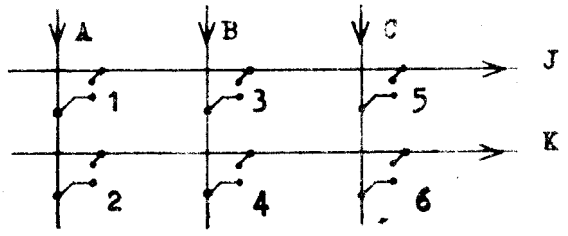
D_1	D_2	D_3	D_4	0 = 74C42 output low	CONTROL
1	0	0	0	2 74C145	Ca1 (N_1) JJ1 Ca2 (N_2) JJ2 Ca3 (N_3) JJ3 Ca4 (N_4) JJ4 Ca5 (N_5)
0	0	0	0	1	Co1 (N_1) LB (N_4) ZB (N_8) Co2 (N_2) SC (N_7) Co3 (N_3)

The truth table for lamps J1, J2, J3 and J4 is:

N_6	N_7	N_8	
1	0	X	JJ1
0	1	X	JJ2
1	1	X	JJ3
0	0	1	JJ4

X = any of the value (0 or 1) is valid.

In this example, we have a 3 x 2 matrix with 6 contacts. To know which is the closed contact, we set A to 1 and reset (0) B and C. Afterwards we look at J and K. If we see two 0's, contacts 1 and 2 are open. If we see 1 at J and 0 at K, contact nº 1 is closed and nº 2 is open a.s.o. Afterwards we do the same with 0's at A and C and 1 at C: With allthese operations, we have checked all contacts, i.e. we have done a matrix operation.
In the machine all these operations are performed 100 times in a second at each column. We have 5 columns, A,B, C,D and E, that operate in the same form as the prior example.
In this case the input rows are: 01,.....08, 01A..... 08A, 03B and 07B. Looking at the wiring schematics, (Space Gambler), we see that column E controlls contacts 12 to 18; column D, 21 to 28; column C, 31 to 38, column B, 42 and 46; column A contacts 54, 57 and 58 and the series 16 to 18 of the double bonus targets
The mission of contact 46 is to give bonus to elevate targets, to take balls and to turn off the lights of the game pannel. The mission of contact 42 is to count the ball changes and to inicializate the fame pannel by lighting die 4 and bonus 1. The rest of the contacts are explained in the schematics. The contacts controlled by the columns C6 and C7 operated in a special way. For example



When C6 is 1 and C7 is 0, the information in 6 passes to 10 and the information in 7 is ignored. When C7 is 1 and C6 is 0, the information in 7 passes to 10 and the information contained in 6 is ignored.
When the switch is open, there are +V volts across the contact and the input is 1. When the switch is closed, there is no voltage across the contact the contact and the input is 0.
IC 4075 is composed by OR gates that permit the concentration of 26 input rows into only 8 rows. These 8 rows are connected to IC 4016 (nº 21 and 22), that are "transparent" to the data bus, when the control signal is 1 and that are in high inpendance state, when the control signal is 0. These control signals come from the I/O control logic. Columns C1 to C6 arealso connected to the output matrix through IC's 4011 and 4081 (nº 18, 19 and 2).

To perform tests and checks in the sound plate, we must follow the following instructions:

N_1	N_2	N_3	N_4	N_5	SOUND
1	0	0	0	1	hundreds (100)
0	1	0	0	1	thousands (1000)
0	0	1	0	1	Tentrhousands (10000)
0	0	0	1	1	hundred thousands (100000)

N5 must always be 1 in order to avoid fading. To check the fading, we set N5 = 0 and the sound will disappear.

The truth table for the cone (Spce Gambler) is:

N_1	N_2	N_3	CONE STAGE
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6

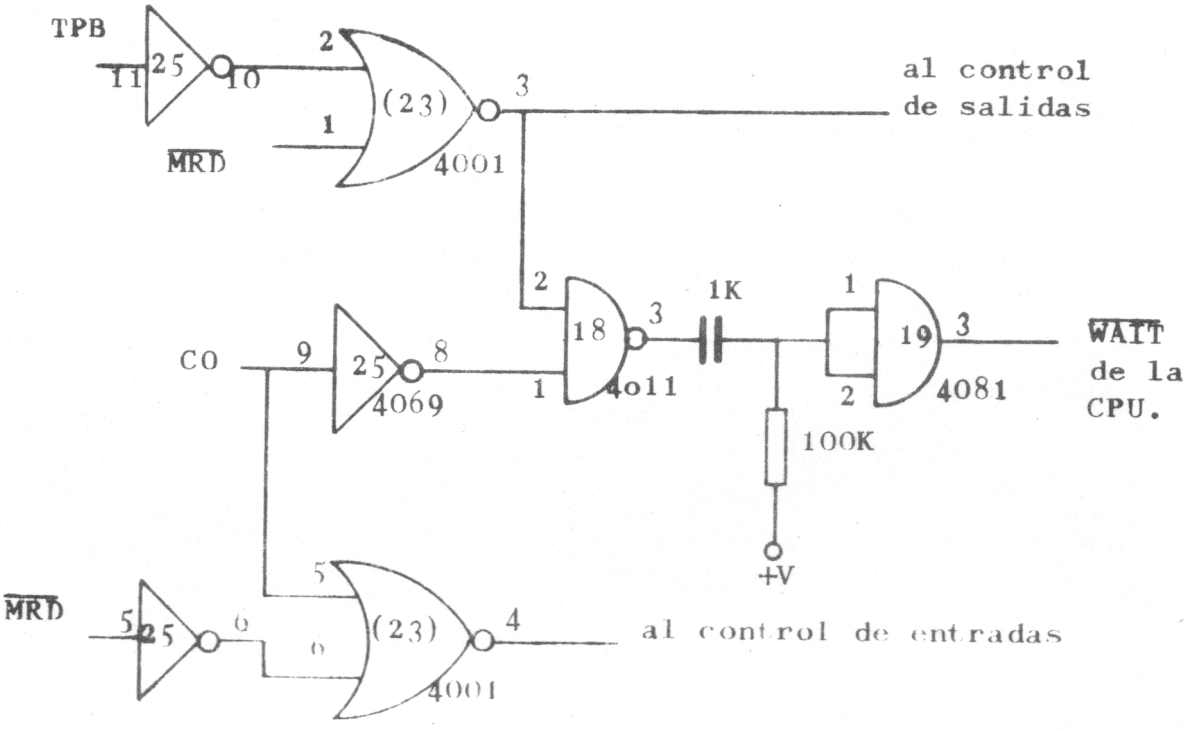
The players, cone and bumper lights are thyristor controlled and their functioning has been already explained, when explainging the cone lights plate.

12.- The MPU plate

Let us study first the inputs organization. For doing that we are foing to use the wiring and MPU schematics.
We see that there are three signals that go out from the CPU (IC nº 28) and go to the decimal decoder, integrated circuit 4028 (nº 20). These signals are NØ, N1 and N2. The decimal decoder decodes the binary number expressed by these three signals and sets the selected output to 1, mantaining the rest of the outputs to 0. The outputs of the decoder are: C0, C1, C2,C3, C4, C5, C6 and C7. Output C0 (pin 3) is selected when the three outputs are 0. This signal is used by the logic that controls the I/O operations. The rest of the outputs C1.. ..C7 ate connected to the input matrix columns and C1 to C6 are also connected to the output matrix columns.

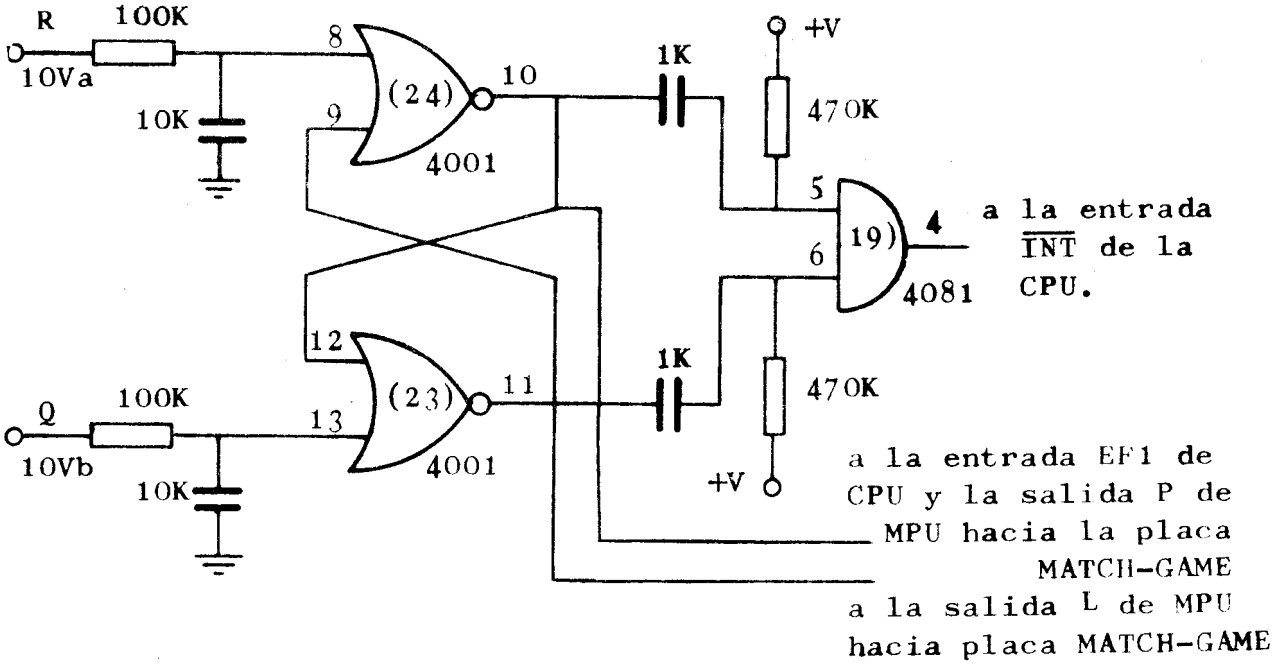
A matrix operated as follows;

The common base of these 6 control gates of the output columns, comes from the I/O control logic and in order to allow the outputs to operate, has to be 1. The first column has a decoder-latch-driver type 4511, similar to the ones in the displays plate and a 40 B flip-flop, that provide signals a, b, c, d, e, f, g, 01 and 1P respectively to the match-game plate. The second column has two latches 4042 and provides signals N1.....N8 to the decoder. They also provide outputs 1A.....8A that go to the plays selection by coin switches of the first and second coin-keeper, located in the MPU. The common of these switches are connected to inputs 25 and 35, that correspond to column C7. The third column is composed if 4 NANO gates of IC 4011 (nº 16) and provide outputs D1, D2, D3 and D4 to the decoder.
Columns 4,5 and 6 are composed of 24 AND gates of 6 integrated circuits type 4081 (nº 3,4,5,6,7 and 29). These columns provide outputs U1 to U8, V1 to V8 and W1 to W8, that are connected to the thuristors plate. Thes outputs have to operated in the thyristors and this is only possible if the voltages in these outputs is maintained between 60 and 100 nicroseconds. For allowing that, the I/O control logic will generate a signal to force the MPU to the PAUSE state everytime that exists an outout. Outputs are given at a rate of 100 times per second at each column, The I/O control logic is composed by:



Signal CO comes form pin 3 of the IC 4028 (nº 20) and when is 1, indicates that there is no I/O instruction and disable the inputs (or control inputs) and the pauses (WAIT = 1). When there is an I/O operation, CO will be 0 and if the operation is an input MRD will become 1. In this case, we will have 1 at the inputs control, 0 at the outputs control and the monostable will not operate as the output nº 1 of the IC nº 18 is 1.

If the I/O operation is an output operation, MRD will be 0, the inputs control will be 0 and the output control will be 1, when TPB is 1. We will have 0 also at output 3 of IC nº 18. This forces the output 3 of IC nº 19 to 0 and the CPU to be in PAUSE state.
The IK capacitor will be charged through the 100K resistor. When the capacitor is completely charged, we will have the input of IC 19 high, forcing the CPU to the state of RUN. This pause has a duration of 60 to 100 microseconds, that is the time necessary to charge the capacitor.
The circuit:



provides a 100 Hz wave that asks for interrupts to the CPU in order to perform I/O operations. These circuits produce also two 50 Hz square waves, that are the control signals for the match-game plate (L and P).
One of the signals goes to EF1, providing to the CPU information of the half cycle of the moment, in order to gice the corresponding informations.
If the game light of a machine sparkle, the resistors of 470K can be changed by other resistors of 1M to increase the raise time.
The circuit composed by the three NAND gates of IC 4011 (nº 32), the transistor and the associated capacitors maintains a 0 at the CLEAR input during 0,5 seconds after the machine is set into operation, to permit the stabilization of the system.
There are three power supplies of +12V, +5V and -5V for the EPROM memories plates (preseries) and a single power supply for the plates with ROM memories (series).
Input EF3 is the switch of 3 or 5 balls and input EF4 is the switch for free game or extra ball.

The oscillator of the system clock is composed by two inverters of IC 4069 (nº 25), together with a 10K resistor and a 82 pF capacitor. The oscillating frecuency is approximately 400 KHz.
The memories used by the system are: two chips of ROM memories (EPROM in the preseries) of 1KB and two RAM chips of 32 bytes each. One of these RAM chips is supplied through a 2200 uF capacitor, when the machine is disconnected. This chip contains the information that can be read and controlled by the push buttons of the door of the machines and by the accumulated games.
Tht totak memory we have, is: 2Kbytes ROM and 64 bytes RAM. So, we need 12 bits to address the memory. As the bus has only 8 lines, we are going to use a four bits latch, IC 4042 (nº 24), to store the four lower weight bits of the higher weight byte of the address. This is so, because the CPU takes out first the 8 bits of higher weight and, then, the 8 of lower weight.
We use the signal TPA as clock for this latch, to pass these four bits from input to output. With these 12 bits and the circuit composed by the dates AND and NAND from IC's nºs. 31, 32, and 19, the memory addressing logic is implemented.
A chip is selected, when its input CS is 0.
To perform a chip select, we use the two higher order bits and signal MRD. The other 10 bits are used to select the position inside of the chip.
For the RAM memories, we must use MWR also, as we must indicate if we want to write in the memory.
If there were problema with the memorization when the machine is disconnected, it is possible to put two 10K resistors between pins 16 and 17 of RAM B (nº 33) and ground (pin 9 of IC nº 33) and another resistor, also of 10K, between pins 1 and 7 of IC nº 32. If there were problems of too quick discharge of the supply capacitor for the RAM memory, we can put a 4K7 resistor between positive and ground of the filter capacitor of 2.200 uF in the power supply of the MPU plate. (For the series machines all these corrections are made in the factory).

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User manual for the CDP 1802 COSMAC microprocessor. By RCA.
Manual de instrucciones "Spce Gambler" - by Playmatic